WHAT IS CLAIMED IS:

1. An integrated circuit package comprising:

a substrate having an opening, first and second surfaces and an outline;

a plurality of routing strips being integral with said substrate;

a plurality of pads disposed on said first surface, at least one of said pads being electrically connected with at least one of said routing strips;

a chip adhered to said second surface of said substrate, said chip having an outline that is substantially the same as said outline of said substrate, said chip having at least one bonding pad;

wire bonding electrically connecting said at least one bonding pad to at least one of said routing strips; and

potting material filling said opening to cover said wire bonding and said at least one bonding pad.

2. The integrated circuit package as recited in claim 1 wherein said substrate includes at least one bus bar being integral with said substrate, said at least one bus bar electrically connected to at least one of said bonding pads and at least one said pads disposed on said first surface of said substrate.

3. The integrated circuit package as recited in claim 1 wherein said substrate includes at least one bus bar being integral with said substrate.

4. The integrated circuit package as recited in claim 1 further comprising at least one solder ball disposed on at least one of said pads disposed on said first surface of said substrate.

5. The integrated circuit package as recited in claim 1 further comprising a mass of solder disposed on at least one of said pads disposed on said first surface of said substrate.

6. The integrated circuit package as recited in claim 1 wherein said substrate comprises a thin sheet.

7. The integrated circuit package as recited in claim 1 wherein said substrate comprises one or more layers, each less than 0.5 mm thick.

8. An integrated circuit package comprising:

an interposer having an opening, first and second surfaces and an outline;

a plurality of bonding terminals on said interposer;

a plurality of connection terminals disposed on said first surface, at least one of said connection terminals being electrically connected with at least one of said bonding terminals;

a chip adhered to said second surface of said interposer, said chip having an outline that is substantially the same as said outline of said interposer, said chip having at least one contact;

wire bonding electrically connecting said at least one contact to at least one of said bonding terminals; and

encapsulating material filling said opening to cover said wire bonding and said at least one contact.

9. The integrated circuit package as recited in claim 8 wherein said interposer includes at least one bus bar.

10. The integrated circuit package as recited in claim 8, wherein said connection terminals include central terminals.

11. The integrated circuit package as recited in claim 8 wherein said interposer includes at least one bus bar, said at least one bus bar electrically connected to at least one of said contacts.

12. The integrated circuit package as recited in claim 11, wherein said bus bar is electrically connected to at least one of said connection terminals .

13. The integrated circuit package as recited in claim 8 wherein said interposer includes at least one electrically conductive layer, said at least one electrically conductive layer being electrically connected to at least one of said contacts.

14. The integrated circuit package as recited in claim 13, wherein said electrically conductive layer is electrically connected to at least one of said connection terminals.

15. The integrated circuit package as recited in claim 8 further comprising at least one solder ball disposed on at least one of said connection terminals

16. The integrated circuit package as recited in claim 8 further comprising a mass of solder disposed on at least one of said connection terminals.

17. The integrated circuit package as recited in claim 8 wherein said interposer comprises a thin sheet.

18. The integrated circuit package as recited in claim 8, wherein said interposer has a plurality of layers.

19. The integrated circuit package as recited in claim 18 wherein each layer of said plurality of layers is less than 0.5 mm thick.

20. The integrated circuit package as recited in claim 18, wherein said bonding terminals are disposed between two layers of said plurality of layers of said interposer.

21. The integrated circuit package as recited in claim 18, wherein said bonding terminals are integral with said interposer.

22. An integrated circuit package comprising:

a substrate having an opening, first and second surfaces and an outline;

a plurality of routing strips being integral with said substrate;

a plurality of pads disposed on said first surface, at least one of said pads being electrically connected with at least one of said routing strips;

a chip adhered to said second surface of said substrate, said chip having an outline that is substantially the same as said outline of said substrate, said chip having at least one bonding pad;

wire bonding electrically connecting said at least one bonding pad to at least one of said routing strips;

at least one bus bar being integral with said substrate, said at least one bus bar electrically connected to at least one of said bonding pads and at least one said pads disposed on said first surface of said substrate;

potting material filling said opening to cover said wire bonding and said at least one bonding pad; and

at least one solder ball disposed on at least one of said pads disposed on said first surface of said substrate.

23. The integrated circuit package as recited in claim 22 further comprising a mass of solder disposed on at least one of said pads disposed on said first surface of said substrate.

24. The integrated circuit package as recited in claim 22 wherein said substrate comprises a thin sheet.

25. The integrated circuit package as recited in claim 22 wherein said substrate comprises one or more layers, each less than 0.5 mm thick.

26. An integrated circuit package comprising:

an interposer having an opening, first and second surfaces and an outline;

a plurality of bonding terminals on said interposer;

a plurality of connection terminals disposed on said first surface, at least one of said connection terminals being electrically connected with at least one of said bonding terminals;

a chip adhered to said second surface of said interposer, said chip having an outline that is substantially the same as said outline of said interposer, said chip having at least one contact;

wire bonding electrically connecting said at least one contact to at least one of said bonding terminals;

at least one electrically conductive layer on said interposer;

encapsulating material filling said opening to cover said wire bonding and said at least one contact; and

at least one solder mass disposed on at least one of said connection terminals.

27. The integrated circuit package as recited in claim 26, wherein said at least one electrically conductive layer is electrically connected to at least one of said at least one contact.

28. The integrated circuit package as recited in claim 27, wherein said electrically conductive layer is electrically connected to at least one of said connection terminals.

29. The integrated circuit package as recited in claim 26 wherein said connection terminals include central terminals.

30. The integrated circuit package as recited in claim 26 wherein said interposer comprises a thin sheet.

31. The integrated circuit package as recited in claim 26, wherein said interposer has a plurality of layers.

32. The integrated circuit package as recited in claim 31 wherein said each layer of said plurality of layers is less than 0.5 mm thick.

33. The integrated circuit package as recited in claim 31, wherein said bonding terminals are disposed between two layers of said plurality of layers of said interposer.

34. The integrated circuit package as recited in claim 31, wherein said bonding terminals are integral with said interposer.